Electronics part B

Dr. ZAINAB KUBBA

FIELD-EFFECT TRANSISTORS (FETS)

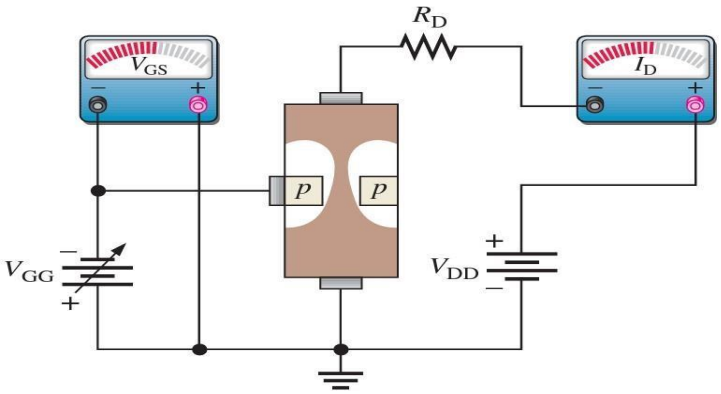
FETs are unipolar devices because, unlike BJTs that use both electron and hole current, they operate only with one type of charge carrier.

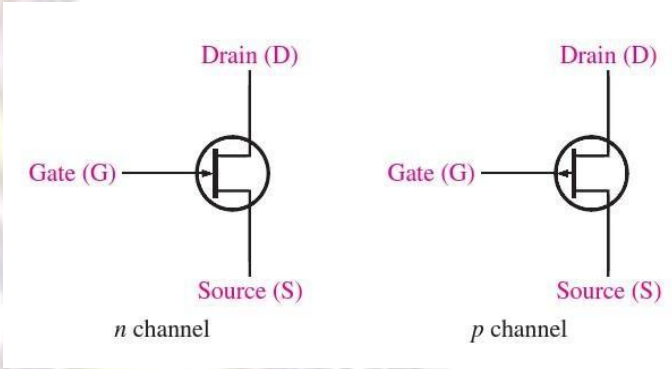
The two main types of FETs are the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET). The term field-effect relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminals (gate).

Recall that a BJT is a current-controlled device; that is, the base current controls the amount of collector current. A FET is different. It is a voltage controlled device, where the voltage between two of the terminals (gate and source)controls the current through the device.

A major advantage of FETs is their very high input resistance. Because of their nonlinear characteristics, they are generally not as widely used in amplifiers as BJTs except where very high input impedances are required. However, FETs are the preferred device in low-voltage switching applications because they are generally faster than BJTs when turned on and off. The IGBTis generally used in high-voltage switching applications.

BASIC OPERATION





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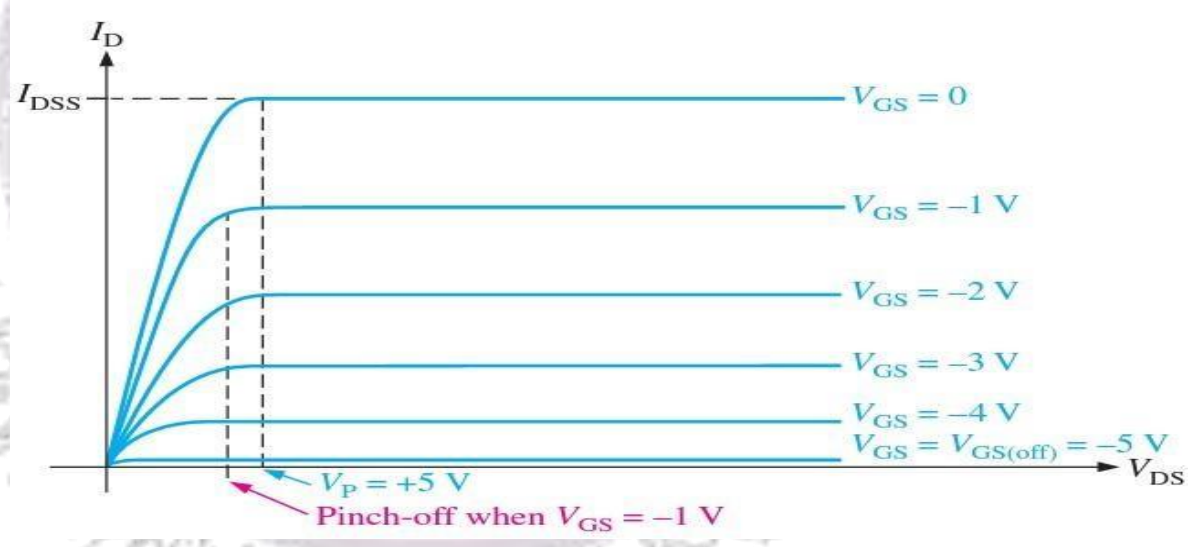
Pinch-Off

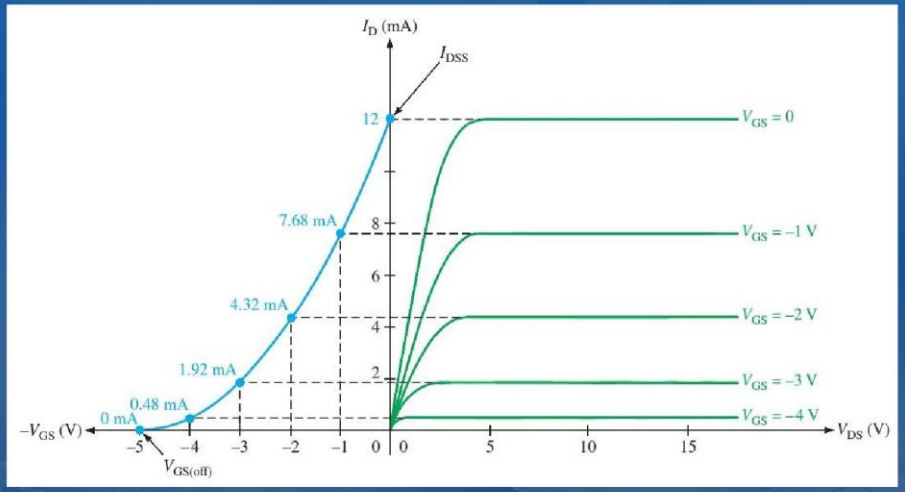
Voltage For VGS 0 V, the value of VDS at which ID becomes essentially constant is the pinch off voltage, VP.For agiven JFET, VP has a fixed value. As you can see, a continued increase in VDS above the pinch off voltage produces an almost constant drain current. This value of drain current is IDSS (Drain to Source current with gate Shorted) and is always specified on JFET datasheets. IDSS is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition



VGS Controls ID Let's connect a bias voltage, VGG, from gate to source As VGS is set to increasingly more negative values by adjusting VGG, a family of drain characteristic curves is produced, Notice that ID decreases as the magnitude of VGS is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in VGS, the JFET reaches pinch-off (where constant current begins) at values of VDS less than VP. The term pinch-off is not the same as **Breakdown**

Cutoff Voltage The value of VGS that makes ID approximately zero is the cutoff voltage, VGS(off). The JFET must be operated between VGS =0 V and VGS(off). For this range of gate-to-source voltages, ID will vary from a maximum of IDSS to a minimum of almost zero. As you have seen, for an channel JFET, there negative VGS is, the smaller ID be-comes in the active region. When VGS has a sufficiently large negative value, ID is reduced to zero. This cut off effect is caused by the widening of the depletion region to a point where it completely closes the channel

JFET UNIVERSAL TRANSFER CHARACTERISTIC



A JFET transfer characteristic curve is expressed approximately as

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Midpoint Bias It is usually desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. Under signal conditions, midpoint bias allows the maximum amount of drain current swing between I_{DSS} and 0. For Equation 8–1, it can be shown that I_D is approximately one-half of I_{DSS} when $V_{GS} = V_{GS(off)}/3.4$. The derivation is given in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS(off)}/3.4}{V_{GS(off)}}\right)^2 = 0.5I_{DSS}$$

So, by selecting $V_{GS} = V_{GS(off)}/3.4$, you should get a midpoint bias in terms of I_D.

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop. Choose R_G arbitrarily large to prevent loading on the driving stage in a cascaded amplifier arrangement. Example 8–9 illustrates these concepts.

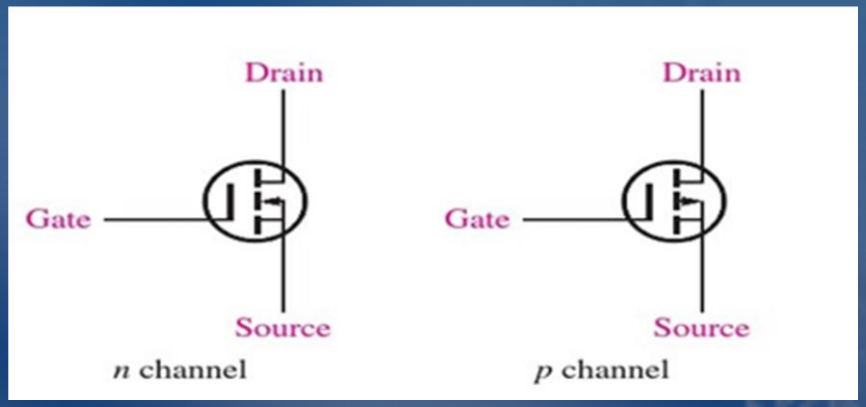
MOSFET

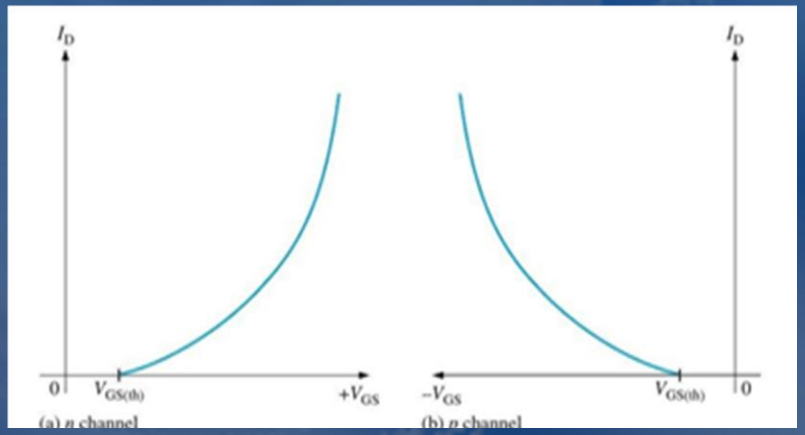
METAL OXID SEMICONDUCTOR FIELD EFFECT TRANSISTOR)

Has no pn junction structure; Instead, the gate of the MOSFET is insulated from the channel by a sicon dioxide (SiO2) layer.The two basic types of MOSFETs are Enhancement(E)and depletion(D)

- Enhancement MOSFET (E-MOSFET)

a For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the ,substrate region adjacent to the SiO2 layer





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Example

The data sheet for a 2N7002 E-MOSFET gives ID(on) = 500 mA (minimum)

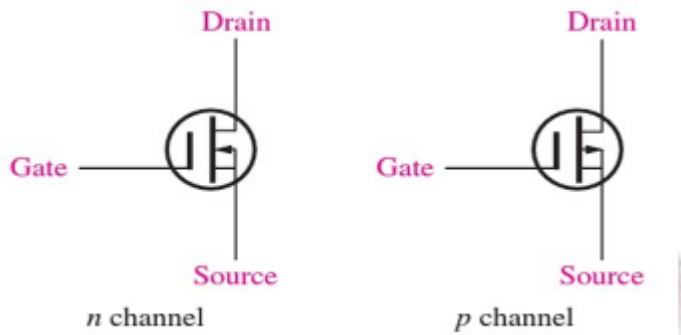
at VGS 10 V and VGS(th) 1 V. Determine the drain current for VGS

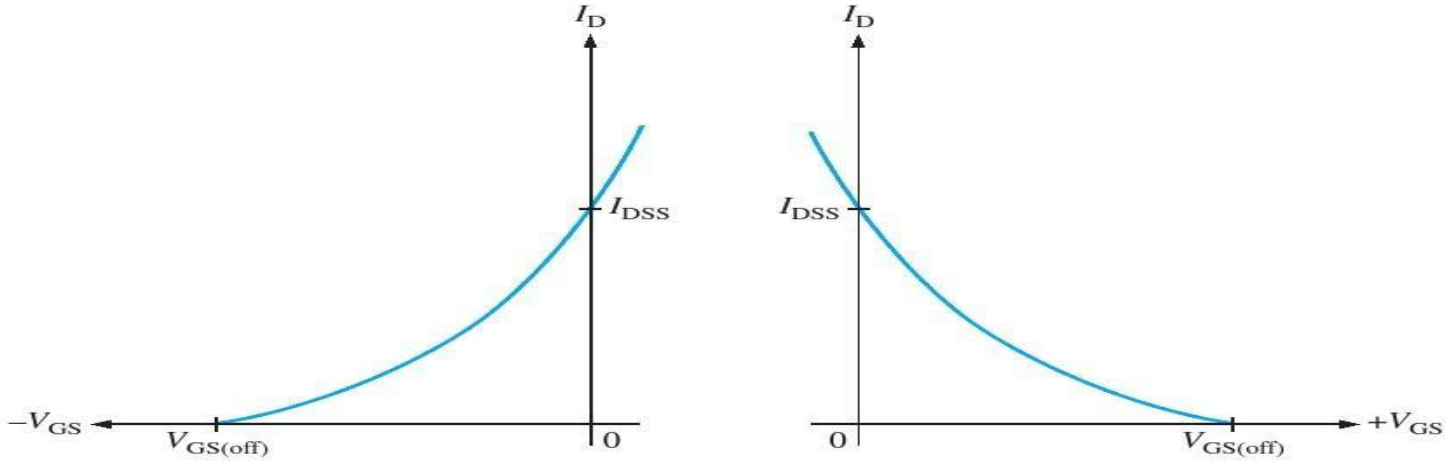
$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

D-MOSFET TRANSFER CHARACTERISTIC





EXAMPLE

For a certain D-MOSFET, $I_{DSS} = 10\text{ mA}$ and $V_{GS(off)} = -8\text{ V}$.

(a) Is this an *n*-channel or a *p*-channel?

(b) Calculate I_D at $V_{GS} = -3\text{ V}$.

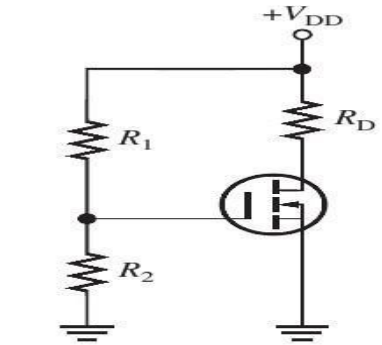
(c) Calculate I_D at $V_{GS} = +3\text{ V}$.

(a) The device has a negative $V_{GS(off)}$; therefore, it is an ***n*-channel** MOSFET.

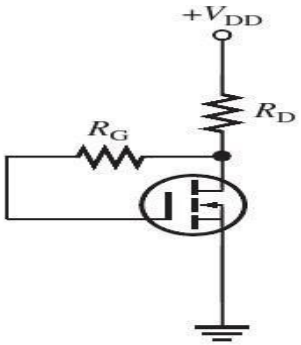
(b) $$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\text{ mA})\left(1 - \frac{-3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{3.91\text{ mA}}$$

(c) $$I_D \cong (10\text{ mA})\left(1 - \frac{+3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{18.9\text{ mA}}$$

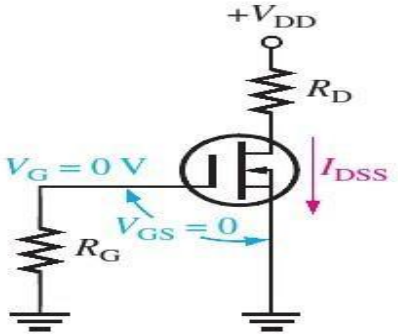
MOSFET BIASING



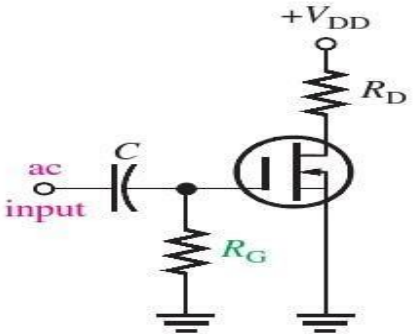
(a) Voltage-divider bias



(b) Drain-feedback bias



(a)



(b)

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$V_{GS} = 0, I_D = I_{DSS}$ as indicated. The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

Dr. Zainab Kubba

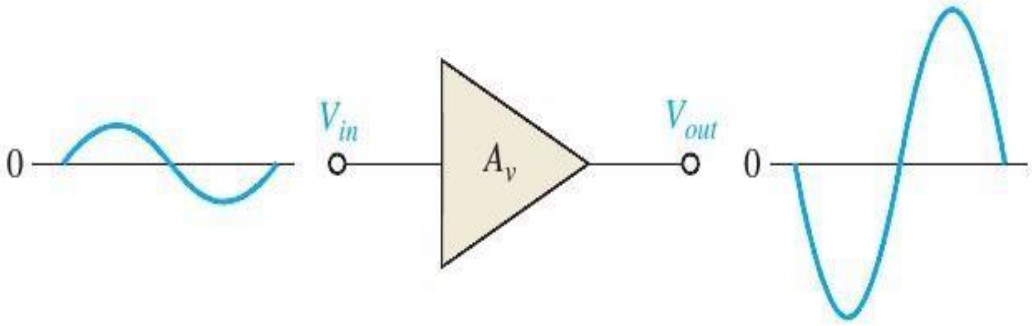
POWER AMPLIFIER

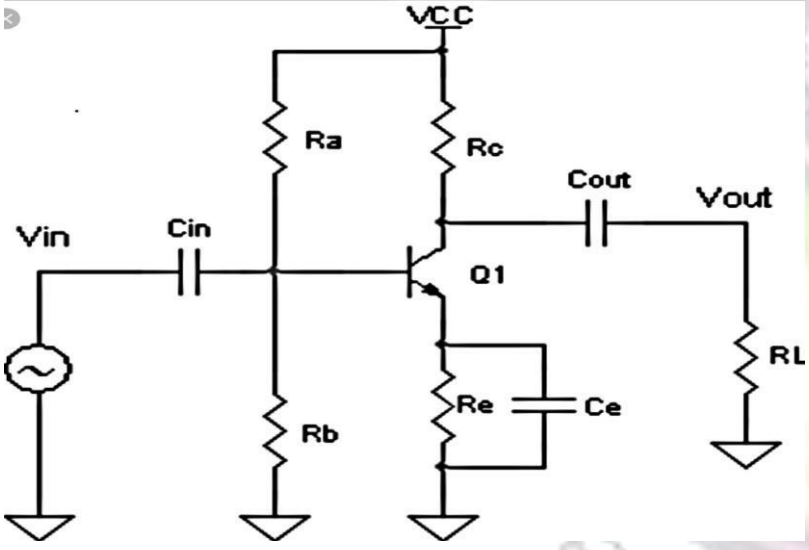
power Amplifier

. Power amplifiers are large-signal amplifiers. This generally means that a much larger portion of the load line is used during signal operation than in a small-signal amplifier. In this chapter, we will cover four classes of power amplifiers: class A, class B, class AB, and class C. These amplifier classifications are based on the percentage of the input cycle for which the amplifier operates in its linear region. Each class has a unique circuit configuration because of the way it must be operated. The emphasis is on power amplification. Power amplifiers are normally used as the final stage of a communications receiver or transmitter to provide signal power to speakers or to a transmitting antenna. BJTs are used to illustrate power amplifier principles

Class A

Com.E, com B or com.C are biased such that it operates in the linear region for 360





from Q point to saturation

$$\triangle I_C = \frac{\triangle V_{CE}}{R_c \| R_L} = \frac{V_{CEQ}}{R_c \| R_L}$$

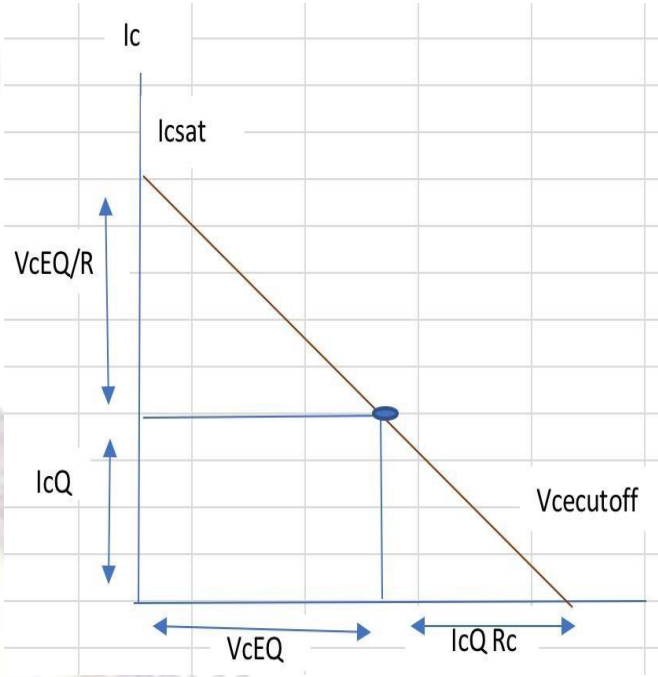
The max.ac collector current I_{csat}

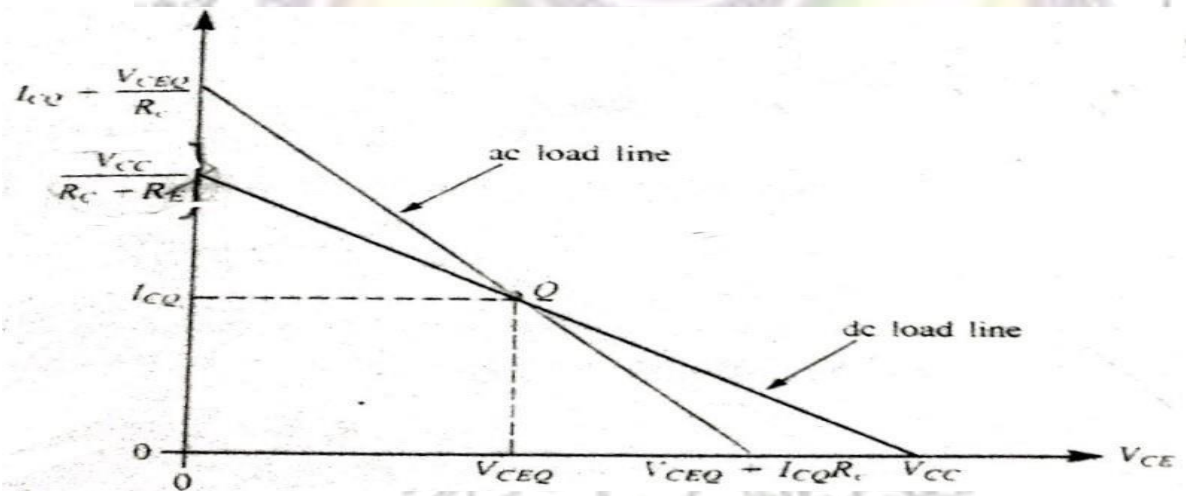
$Ic(sat) = I_{CQ} + \triangle I_C$

From Q point to cutoff

$$\triangle V_{CE} = \triangle I_C \times R_c \| R_L = I_{CQ} \times R_c \| R_L$$

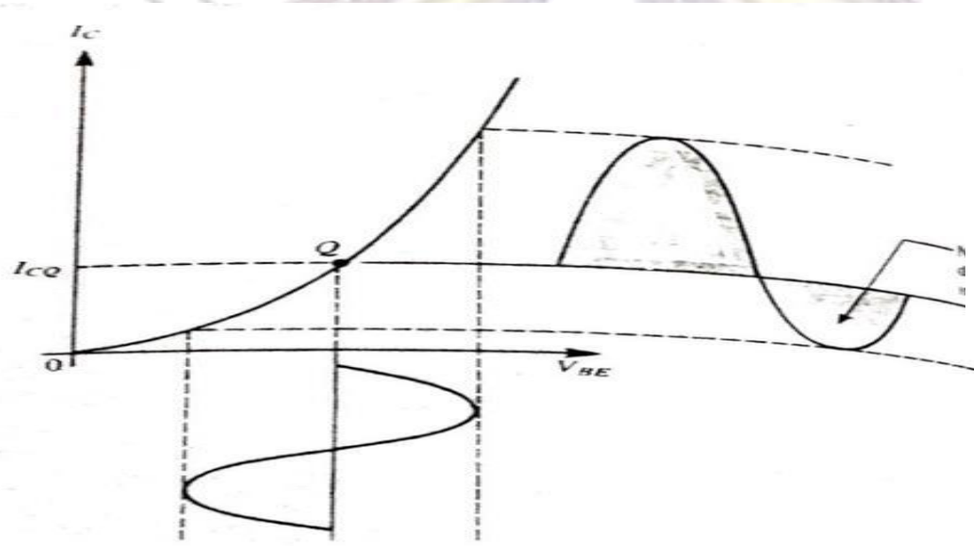
$V_{ce(cutoff)} = V_{CEQ} + \triangle V_{CE}$





Nonlinear distortion

When the collector current swing over a large portion of the transconductance curve. Distortion can occur on the negative half cycle. This is caused by the greater nonlinearity on the lower end of the curve as shown in the figure. This distortion can be sufficiently reduced by keeping the collector current on the more linear part of the curve at higher values of ICQ and VBEQ



Nonlinear distortion

Efficiency

The efficiency of any amplifier is the ratio of the output signal supplied to a load to-the total power from the dc supply. The maximum output signal power that can be obtained as in

$$P_{out(max)} = (0.707I_c)(0.707V_c)$$

$$P_{out(max)} = 0.5I_{CQ}V_{CEQ}$$

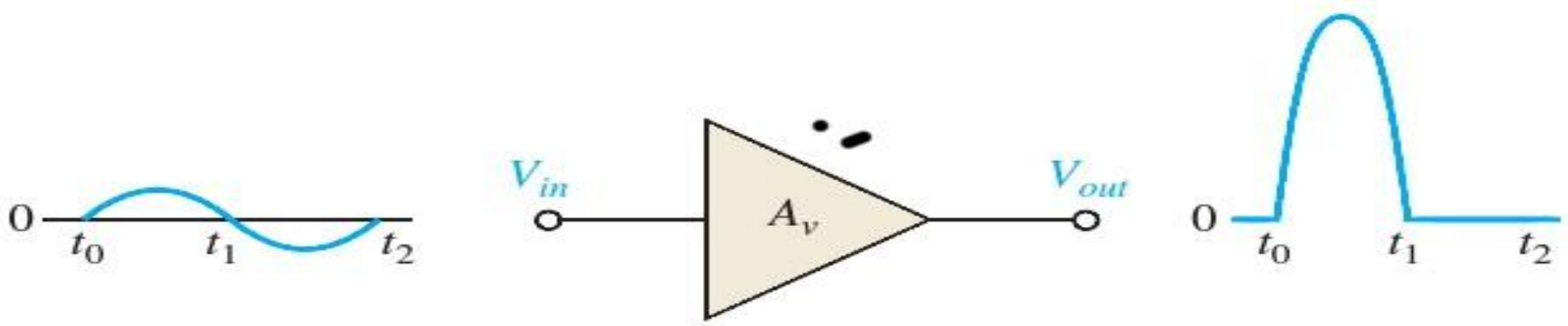
The maximum efficiency, of a capacitively coupled class A amplifier is

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.5I_{CQ}V_{CEQ}}{2I_{CQ}V_{CEQ}} = 0.25$$

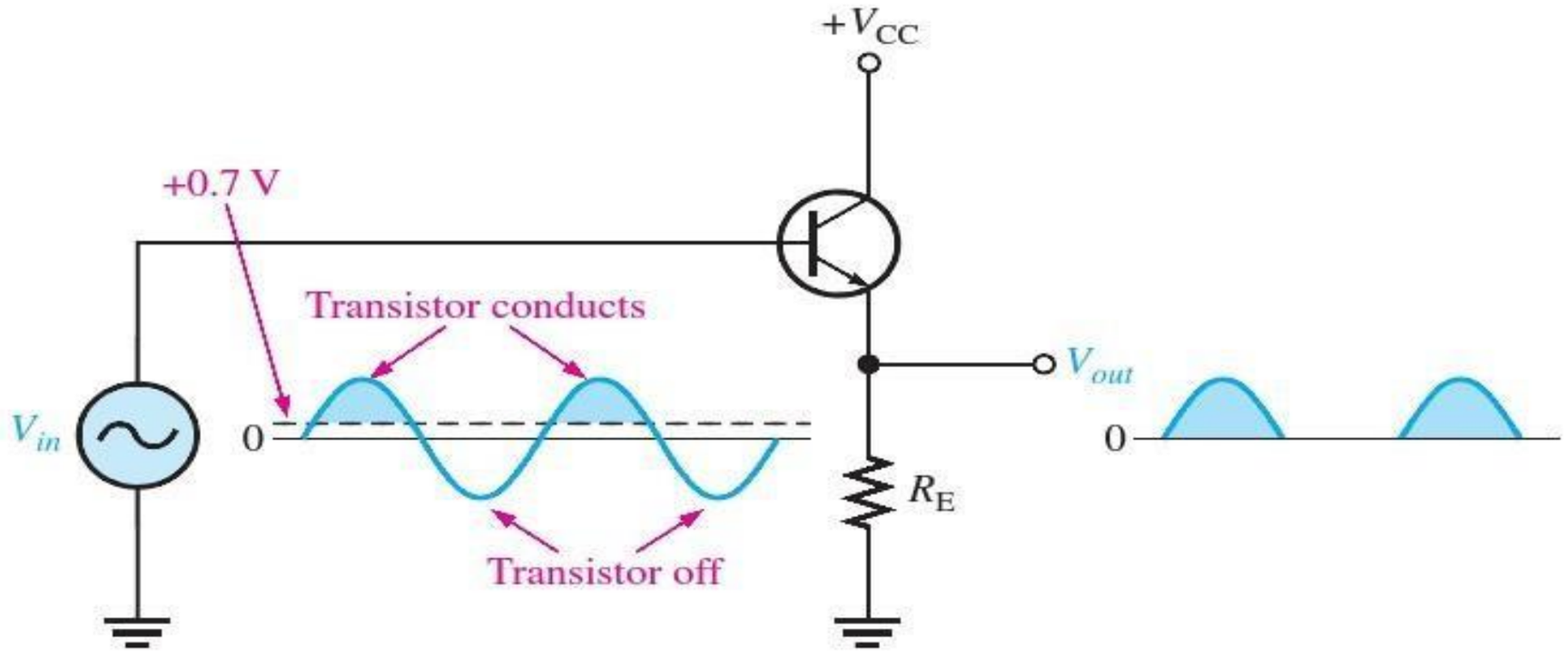
The maximum efficiency of a capacitively coupled class A amplifier cannot be higher than 0.25, or 25%, and, in practice, is usually considerably less (about 10%).

Class B

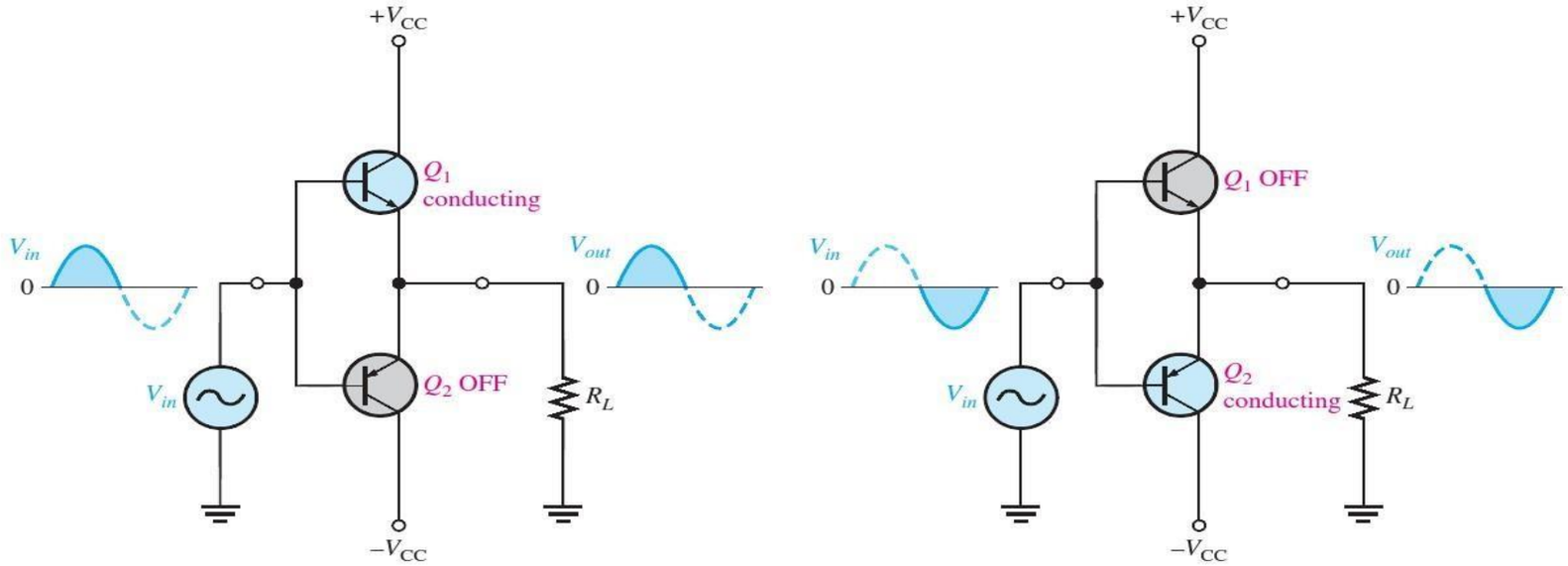
The class B amplifier is biased at the cutoff point so that It is brought out of cutoff and operates in its linear region. the input signal drives the transistor into conduction where, the output is not a replica of the input



As you can see, the circuit in the figure only conducts for the positive half of the cycle. To amplify the entire cycle, it is necessary to add a second class B amplifier that operates on the negative half of the cycle. The combination of two class B amplifiers working together is called push-pull operation.



Push-pull Amplifier

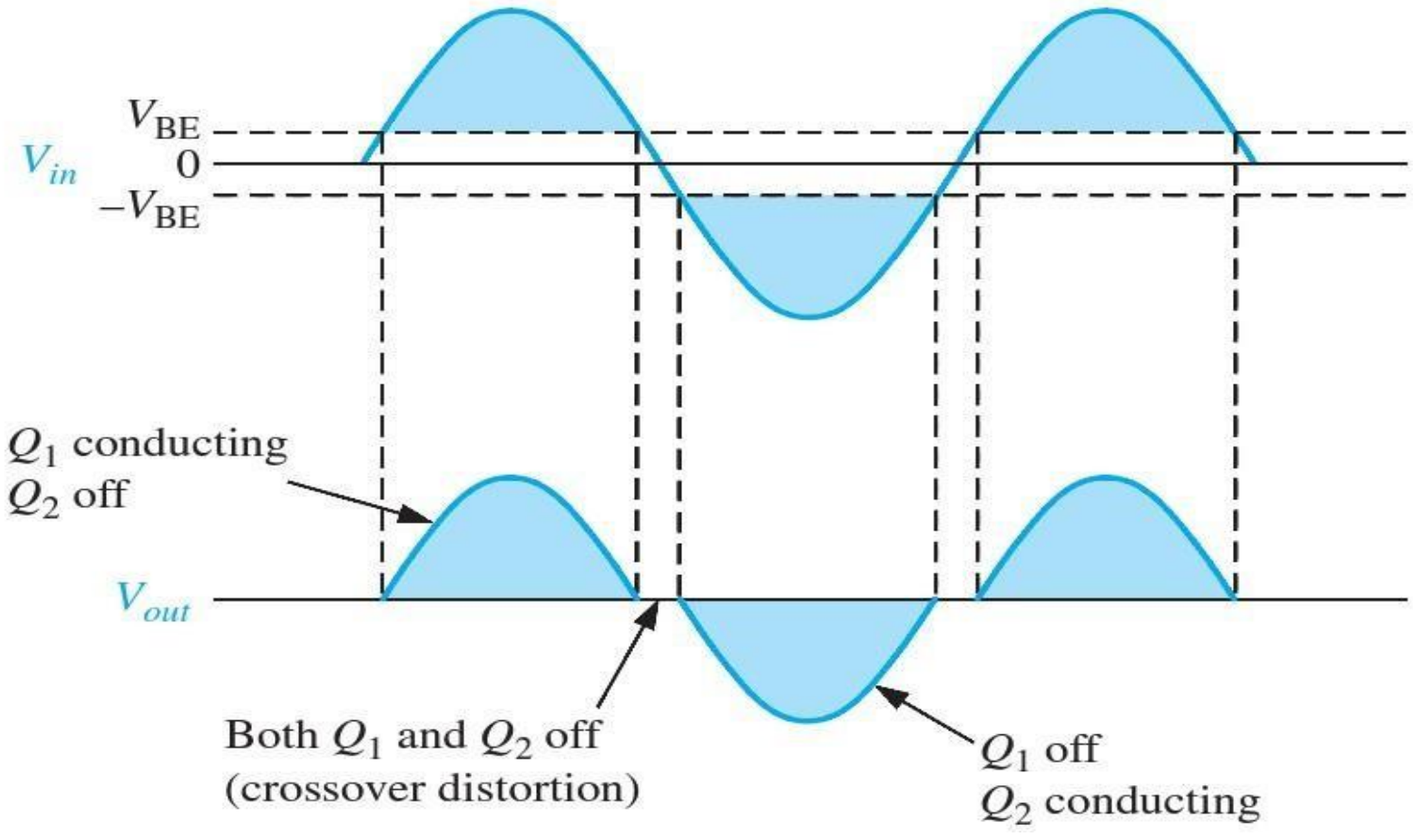


(a) During a positive half-cycle

(b) During a negative half-cycle

Crossover Distortion

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed VBE before a transistor conducts. Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting. The resulting distortion in the output waveform is called crossover distortion



Efficiency An advantage of push-pull class B and class AB amplifiers over class A is a much higher efficiency. This advantage usually overrides the difficulty of biasing the class AB push-pull amplifier to eliminate crossover distortion. Recall that efficiency, η is defined as the ratio of ac output power to dc input power.

$$\eta = \frac{P_{out}}{P_{DC}}$$

The maximum efficiency, η_{max}, for a class B amplifier (class AB is slightly less) is developed as follows, starting with Equation 7–6.

$$P_{out} = 0.25 I_{c(sat)} V_{CC}$$

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.25 I_{c(sat)} V_{CC}}{I_{c(sat)} V_{CC}/\pi} = 0.25\pi$$

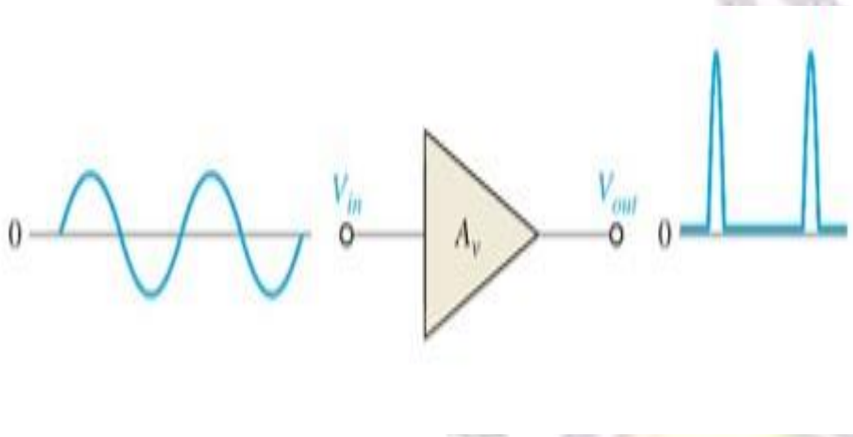
$$\boldsymbol{\eta_{max} = 0.79}$$

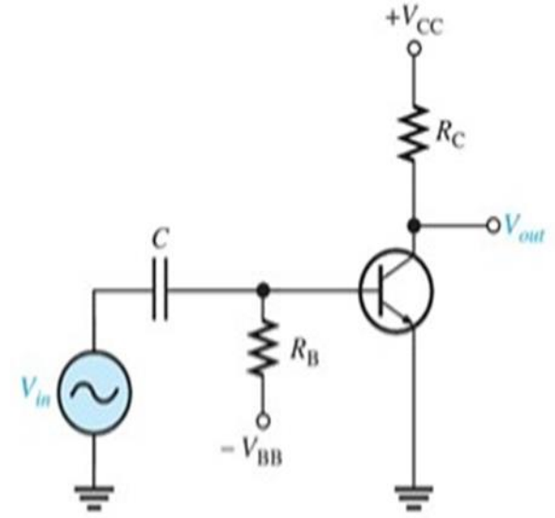
or, as a percentage,

$$\eta_{max} = 79\%$$

Recall that the maximum efficiency for class A is 0.25 (25 percent).

Class C amplifier





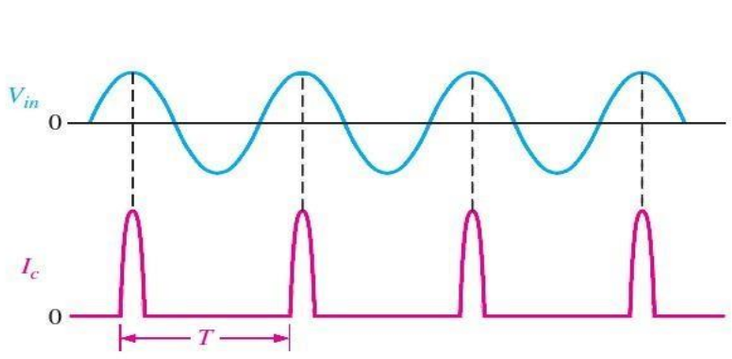
(a) Basic class C amplifier circuit

Power Dissipation

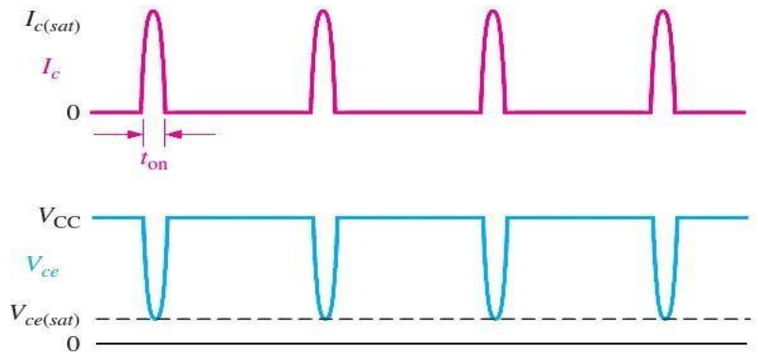
$$P_{D(on)} = I_{c(sat)} V_{ce(sat)}$$

The transistor is on for a short time, ton, and off for the rest of the input cycle. Therefore, assuming the entire load line is used, the power dissipation averaged over the entire cycle is

$$P_{D(avg)} = t_{on}/T \; P_{D(on)} = t_{on}/T \; I_{c(sat)} V_{ce(sat)}$$



(a) Collector current pulses



(b) Ideal class C waveforms

Maximum Output Power

Since the voltage developed across the tank circuit has a peak-to-peak value of approximately $2V_{CC}$, the maximum output power can be expressed as

$$P_{out} = \frac{V_{rms}^2}{R_c} = \frac{(0.707V_{CC})^2}{R_c}$$

$$\boldsymbol{P_{out} = \frac{0.5V_{CC}^2}{R_c}}$$

R_c is the equivalent parallel resistance of the collector tank circuit at resonance and represents the parallel combination of the coil resistance and the load resistance. It usually has a low value. The total power that must be supplied to the amplifier is

$$P_T = P_{out} + P_{D(avg)}$$

Therefore, the efficiency is

$$\boldsymbol{\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}}}$$

When $P_{out} >> P_{D(avg)}$, the class C efficiency closely approaches 1 (100 percent).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